APPLICATION
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Applicant:

Omer H. Dokumaci, et al.

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"Self-aligned Double-Gate Process by Self-aligned Oxidation"

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INTERNATIONAL BUSINESS MACHINES CORPORATION
ARMONK, NEW YORK 10504

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Self-aligned Planar Double-Gate Process by Self-aligned Oxidation

TECHNICAL FIELD

The field of the invention is that of forming dual-gate transistors in integrated circuit processing, in particular self-aligned dual gate transistors.

BACKGROUND OF THE INVENTION

Workers in the field of integrated circuits are constantly striving to reduce the size of devices, in particular transistors.

As FET dimensions are scaled down, it becomes increasingly difficult to control short-channel effects by conventional means. Short-channel effects well known to those skilled in the art are the decrease in threshold voltage Vt, in short-channel devices, i.e. sub-0.1 micron, due to two-dimensional electrostatic charge sharing between the gate and the source/drain region.

An evolution beyond the standard single gate metal oxide semiconductor field effect transistor (MOSFET) is the double-gate MOSFET, in which the device channel is confined between top and bottom gate dielectric layers.

This structure, with a symmetrical gate structure, can be scaled to about half of the channel length as compared with a conventional single gate MOSFET structure. It is well known that a dual gate or double-gate MOSFET device has several advantages over conventional single gate MOSFET devices. Specifically, the advantages over conventional single gate counterparts include: a higher transconductance, and improved short-channel effects.

For instance, Monte Carlo simulation has been carried out on a 30nm channel dual-gate MOSFET device and has shown that the dual gate device has a very high transconductance (2300mS/nm) and fast switching speeds (1.1ps for nMOSFET).

Moreover, improved short channel characteristics are obtained down to 20nm channel length with no doping needed in the channel region. This circumvents the tunneling breakdown, dopant quantization, and dopant depletion problems associated with channel doping that are normally present with single gate MOSFET devices.

Currently, both vertical and horizontal gate structures are actively being pursued by many workers in the field. The horizontal gate structure has several advantages over the vertical structures due to the similarity of current state of the art CMOS devices. However, one major and formidable challenge of fabricating the double gate is aligning the bottom gate to the top gate.

SUMMARY OF THE INVENTION

The invention relates to an integrated circuit having dual-gate transistors.

An aspect of the invention is the formation of a self-aligned back gate by oxidizing a portion of the back gate electrode layer using the front gate as an oxidation mask.

Another aspect of the invention is the implantation at the outer edges of the structure of a species that promotes oxidation.

Another aspect of the invention is the oxidation for a sufficient time and temperature to reduce stress in the transistor body.

Another aspect of the invention is the transverse extent of the oxidation to extend the boundary of the back gate below the edge of the transistor body.

Another aspect of the invention is the formation of raised source and drain structures within a space left by the spacers that define the width of the transistor body.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A and 1B show steps in the formation of the original unpatterned

structure.

Figure 2 shows a front gate electrode.

Figure 3 shows the formation of a first pair of spacers defining the transistor body.

Figure 4 shows the result of etching the SOI layer to define the transistor body.

Figure 5 shows the formation of a second pair of spacers that protect the transistor body during oxidation.

Figure 6 shows the result of the oxidation that defines the width of the back gate electrode.

Figure 7 shows the result of depositing dielectric enclosing the transistor structure.

Figure 8 shows the result of stripping the spacers to form an aperture holding the raised S/D structures.

Figure 9 shows the raised S/D contacts with isolating dielectric to insulate the S/D contacts.

DETAILED DESCRIPTION

Figure 1A shows an initial SOI wafer having bulk substrate 105, with buried oxide (BOX) 107 separating the bulk substrate from the single-crystal silicon SOI layer 4 that will become the transistor body. Layer 4 has a nominal thickness that may range from 2nm to 50nm.

A layer of thermal oxide 3 that will become the back gate dielectric is grown on silicon layer 4 to a thickness of 1nm to 3nm and a layer of polycrystalline silicon (poly) 2 is deposited by CVD in the range of 100nm to 400nm that will become the back gate electrode. Layer 3 may be composed of oxynitride or may be nitridized as a design choice, so long as it is suitable for a gate dielectric.

Figure 1B shows the result of bonding a second, bulk wafer to the first one and removing substrate 105, e.g. by grinding and BOX layer 7, e.g. by etching in dilute hydrofluoric acid. The new substrate is denoted with the numeral 1 in Figure 1B.

Layer 4 is oxidized again with a thermal oxide 5 that will become the front gate dielectric. Layer 5 may also be oxynitride or may be nitridized. It may also optionally be a high dielectric material such as ZrO_2, HfO_2, AlO_2 or other conventional high-k material. Another poly layer 6 is deposited by CVD, preferably in the range of 70nm to 250nm in thickness.

Figure 2 shows the result of depositing on poly layer 6 a pair of first and second pattern transfer layers, illustratively layer 7a of 10nm to 70nm of oxide (SiO_2) and layer 7b of 10nm to 70nm of nitride (Si_3N_4). A layer of photoresist is deposited and patterned to define the front gate. The pattern transfer layers are etched to define a hardmask and the resist is stripped. Poly layer 6 is etched using the hardmask as a pattern to form first (front) gate 8.

Figure 3 shows the result of depositing and defining layers that will protect first gate 8 during the formation of the second or back gate. A conformal oxide layer 9 is deposited, illustratively of CVD TEOS 2nm to 10nm in thickness. Next, a CVD nitride film 10nm to 100nm thick is deposited. The nitride film is etched in a conventional directional etch to remove the film on horizontal surfaces to form nitride spacers 10, stopping the etch on oxide film 9.

Figure 4 shows the result of performing another directional etch on layer 9 and gate layer 5, e.g. with HBr chemistry and a directional etch that removes silicon selectively to oxide (e.g. HBr chemistry) to etch through layer 4, stopping on layer 3. The preceding directional etches are conventional and generically described as reactive ion etches.

The result is that the transistor body has been defined to extend past the first gate electrode on both the left and right in the figure by the thickness of spacers 9 and 10. Spacers 9 and 10 will be referred to as being in proximity

to the gate and to the vertical edge of the transistor body, meaning that they are close to the referenced structure but not necessarily directly in contact with it. Additional liners may be deposited as an etch stop or as an insulator to remain in the final structure. The vertical edge of the transistor body is denoted with numeral 11 in this figure and will be contacted by additional silicon added in a later stage. The thickness of the transistor body perpendicular to the plane of the paper will be set according to the designed current capacity of the transistor, as is conventional.

Optionally, an extra space may be allowed in front of or behind the plane of the paper to make contact with the lower gate electrode that will be formed from layer 2.

Figure 5 shows the result of depositing a conformal layer of CVD nitride and etching it directionally to form spacers 12 that protect the vertical edge of the transistor body and also define the boundary of the area in layer 2 that will be oxidized in the following step.

Illustratively, as shown in Figure 6, the thickness of spacers 10 and 12 are set to facilitate the following oxidation step, in which layer 2 is oxidized through oxide layer 3, so that only the central unoxidized portion functions as the back gate electrode.

Those skilled in the art would not think to exploit the transverse growth of oxide to penetrate under the transistor body because the expansion in volume

of the oxide compared with silicon would have been though to delaminate or to exert undesired stress on the transistor body.

Advantageously, it has been found that the transverse oxide growth is rapid enough in the poly layer 2 that the resulting stress is acceptable. In addition, it has been found that if the oxidation is performed at a temperature of about 1000C or greater for a time of about 20 min or greater, that the stress caused by the oxidation is relaxed since the SiO2 is more viscous under these conditions.

The parameters of the oxidation step are adjusted empirically to provide for the correct amount of sideways growth. Optionally, an angled ion implant of phosphorus or other oxide-promoting species, indicated schematically by arrows 123 in Figure 5 and by shaded area 125, can be used prior to the oxidation to facilitate and control the lateral oxidation extent. The angle with respect to the wafer normal will depend on the height and spacing of nearby structures. The dose and voltage will be set empirically. Greater lateral penetration can be achieved by increasing the voltage.

Alternatively, or additionally, a nitrogen (or other oxide-retarding species) implant, indicated schematically by arrows 127 and shaded area 128 in Figur 5, may be performed at a normal incidence angle. The back gate electrode with a sufficient amount of nitrogen incorporation will retard the oxidation in the vertical direction thereby enabling more control and flexibility over the vertical to lateral oxidation extent. The voltage can be set to leave a light

dose near thetop of layer 2 and a retarding dose in the lower portion.

The oxide penetrates a nominal 30-70nm sideways toward the central portion and a nominal 30-70nm downward.

Figure 7 shows the result of depositing a CVD oxide film 14 to a thickness nominally greater than the height of the gate stack (plus layers 7a and 7b), that is then planarized, e.g. in a chemical-mechanical polishing (CMP) process.

After planarization, the oxide is recessed to a height less than the height of the gate stack (and greater than the height of gate 8).

Figure 8 shows the result of stripping the spacers 10 and 12 and cap 7b, e.g. in hot phosphoric acid, to open an aperture 25 for the raised source-/drain structures. Another nitride spacer 15, having a nominal thickness of 10-70nm , is formed on the vertical surfaces of the aperture to isolate the S/D contacts from the gate. An implant of conventional magnitude for the S/D may be performed in aperture 25 at this time. The completion of the S/D, whether at this time or after the raised S/D step shown in Figure 9, completes the transistor.

A conventional cleaning step (preferably wet cleaning) removes any residue from vertical surfaces 11 of the transistor body to make a good contact between the body and the raised S/D structures.

Figure 9 shows the result of filling aperture 25 with silicon 16 - by selective epitaxy, or by deposition of amorphous silicon or poly (with or without a S/D implant). A planarization, e.g. CMP followed by a dry etch to recess the silicon results in the structure shown, in which apertures 27 are prepared for the deposition of a conventional interconnect to connect transistors to form the circuit.

Conventional middle of the line and back of the line steps are performed to complete the circuit, referred to for convenience as completing the circuit.

The layers that form gate electrodes 2 and 8 are put down with conventional dopant concentrations (or implanted later) sufficient to provide the proper conductivity for the gates. Similarly, the raised S/D structures have the proper amount of dopant added during deposition.

Layer 4 that forms the transistor body may have a conventional dopant concentration. Those skilled in the art are aware of the type and concentration of dopants to form NFETs and PFETs.

Process Flow

Initial Wafer Preparation
- Start with SOI wafer with silicon SOI layer
- Thermal oxide for back gate dielectric
- Poly for back gate electrode

Bond Carrier Wafer
- Remove initial substrate
- Remove initial BOX

Front gate dielectric

Front gate electrode

Gate Patterning
- Pattern transfer layer 1 (oxide)
- Pattern transfer layer 2 (nitride)
- Pattern front gate

First Spacer Formation
- Deposit Etch stop layer
- Deposit Spacer layer
- Directional etch to form spacers

Channel Patterning
- Etch pattern transfer layer 1
- Etch channel, stopping on back oxide

Second Spacer Formation

Deposit spacer material

Define spacers

Define Self-Aligned Back Gate

Oxidize Back Gate Layer, extending oxidation horizontally to define self-aligned gate

Deposit Thick dielectric, planarize

Remove First and Second Spacers

Gate Isolation Spacers

S/D Contact Deposition

While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.